Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) A digital to analog converter (DAC) configured to convert input digital audio data to analog data, the digital audio data having a predetermined input sample rate, the DAC comprising:

a digital processing portion configured to (i) receive as an input the digital audio data and timing information, the timing information being representative of a time base of the input sample rate and (ii) digitally process the digital audio data and the system timing data to produce serialized output data; and

an analog processing portion configured to convert the serialized data to an analog format;

wherein the digital processing portion operates in accordance with at least one system clock having a corresponding system clock rate; and

wherein the at least one corresponding system clock rate ~~rates~~ is independent of ~~asynchronous with~~ the input sample rate.

2. (Original) The DAC of claim 1, wherein the digital processing portion includes a rate manager and a rate converter.

3. (Original) The DAC of claim 2, wherein the rate converter is asynchronous.

4. (Currently Amended) The DAC of claim 2 ~~1~~, wherein the rate manager receives the input sample rate data in accordance with the clock and produces an input sample rate value therefrom.

5. (Original) The DAC of claim 4, wherein the value correlates the input sample rate with a desired output sample rate.

6. (Currently Amended) The DAC of claim 5, wherein the value is a fractional value having ranges from -2^{17} to 2^{17} ~~-217 to 217~~.

7. (Original) The DAC of claim 6, wherein the fractional value is computed each period of the clock.

8. (Original) The DAC of claim 7, wherein the rate converter performs at least one of decimating and interpolating the digital audio data based upon the fractional value.

9. (Original) The DAC of claim 4, wherein the timing information includes system time clock (STC) pulses.

10. (Original) The DAC of claim 4, wherein the digital processing portion is formed on a single integrated circuit chip.

11. (Original) The DAC of claim 4, wherein the rate converter output audio samples at the desirable output sample rate.

12. (Original) The DAC of claim 11, wherein the digital processing portion further comprises a digital (cascaded integrator-comb (CIC)) filter for (i) receiving the output audio samples at the desirable output rate and (ii) up-converting the output audio sample to an intermediate sample rate.

13. (Original) The DAC of claim 12, wherein the digital processing portion further comprises a modulator mapper configured to receive the output audio samples at the intermediate sample rate, the modulator mapper being configured to reduce a noise level of the output audio samples, the modulator mapper producing a quantized output.

14. (Original) The DAC of claim 13, wherein the digital processing portion further comprises a parallel to serial converter configured to (i) receive the quantized output, (ii) produce a serialized output therefrom, and (iii) provide the serialized output to the analog processing portion.

15. (Currently Amended) A method for converting digital audio data having a predetermined input sample rate to analog samples in a digital to analog converter (DAC), the method comprising:

receiving timing information representative of a time base of audio input data, the audio input data having a predetermined input sample rate;

producing an input sample rate value based upon the received timing information, the input sample rate value being representative of the predetermined input sample rate and a desirable output sample rate; and

rate converting the audio input data in a based upon a system clock, the rate converting producing output samples at in accordance with the input sample rate value, the output samples being output at the desirable output sample rate;

wherein the input sample rate is independent of ~~asynchronous with~~ the system clock.

16. (Currently Amended) The method of claim 15 ~~11~~, wherein the rate converting is asynchronous.

17. (Currently Amended) The method of claim 15 ~~11~~, wherein the input sample rate value is a fractional value having ranges from -2^{17} to 2^{17} ~~-217 to 217~~.

18. (Original) The DAC of claim 13, wherein the fractional value is computed each period of the system clock.

19. (Original) The DAC of claim 18, wherein the system clock has a higher rate than the input sample rate.

20. (Currently Amended) An apparatus configured for converting digital audio data having a predetermined input sample rate to analog samples in a digital to analog converter (DAC), the apparatus comprising:

means for receiving timing information representative of a time base of audio input data, the audio input data having a predetermined input sample rate;

means for producing an input sample rate value based upon the received timing information, the input sample rate value being representative of the predetermined input sample rate and a desirable output sample rate; and

means for rate converting the audio input data in a based upon a system clock, the rate converting producing output samples at in accordance with the input sample rate value, the output samples being output at the desirable output sample rate;

wherein the input sample rate is independent of ~~unrelated to~~ the system clock.